#6/C.F.R. DKing 2127/62

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Satoshi TAKANO

Application No.:

09/819,690 10 ADEMAS

Docket No.:

109107

Filed: March 29, 2001

For:

SEMICONDUCTOR MANUFACTURING METHOD, SUBSTRATE PROCESSING

METHOD, AND SEMICONDUCTOR MANUFACTURING APPARATUS

REQUEST FOR CORRECTION OF PALM RECORDS

Director of the U.S. Patent and Trademark Office Washington, D.C. 20231

Sir:

Attached is a photocopy of the original filing receipt on which errors have been corrected in red. These errors are being brought to the attention of the Patent and Trademark Office so that it may correct its records.

Respectfully submitted,

James A. Oliff

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Date: July 30, 2001

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CONFIRMATION NO. 3148

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UPDATED FILING RECEIPT

Date Mailed: 06/28/2

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> NAKANO-KU

Applicant(s)

Satoshi Takano, Tokyo, JAPAN;

Domestic Priority data as claimed by applicant

-) Assignment for Published Patent Application HITACHI KOKUSAI ELECTRIC INC.

Foreign Applications

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Early Publication Request: No

Title

Semiconductor manufacturing method, substrate processing method, and semiconductor manufacturing apparatus

Preliminary Class

438



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** CONTINUING I ** FOREIGN APP JAPAN 200 JAPAN 200	DATA LICA 0-916 01-601		GRANTI	, ED					
Foreign Priority claimed 35 USC 119 (a-d) conditions met Verified and Acknowledged Acknowledged				STATE OR COUNTRY JAPAN			TOTA CLAI 8		INDEPENDENT CLAIMS 5
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